AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Original) A method for reducing pilot tone phase interference at the transmitter in a discrete multi-tone (DMT) communications system comprising:

generating DMT signal segments REVERB and SEGUE with a pseudo-random pattern generator using an initial pattern that minimizes the pilot tone phase offsets in both segments; and

transmitting the above-defined REVERB and SEGUE signals in the DMT initialization sequence.

2. (Original) The method of claim 1, further comprising:

generating ADSL-over-POTS DMT signal segments C-REVERB and C-SEGUE with a pseudo-random pattern generator polynomial as defined by the ADSL standard but using an initial pattern of 90 (0x05A); and

transmitting the C-REVERB and C-SEGUE signal in the DMT ADSL standard initialization sequence.

3-6. (Canceled).

7. (Previously presented) A method for timing recovery at the receiver in a discrete multi-tone (DMT) communications system comprising:

receiving a pilot tone generated and transmitted by an associated far-end transmission unit along with other signal streams at a particular receiver;

converting the plurality of received signals through an analog to digital converter (ADC) to create a digital signal stream;

detecting a cyclic prefix in the received digital signal stream;

zeroing out the received digital signal stream from the input to a timing recovery circuit while the cyclic prefix is present in the received signal stream to create a frequency correction signal; and

using the frequency correction signal to modify the ADC sampling timing.

8. (Previously presented) The method of claim 7, further comprising:

synchronizing a digital to analog converter (DAC) in the transmitting path by using a sampling clock derived from the ADC.

9. (Canceled)

10. (Previously presented) The method of claim 31, further comprising:

synchronizing a digital to analog converter (DAC) in the transmitting path by using a sampling clock derived from the ADC.

11. (Previously presented) A method for timing recovery at the receiver in a discrete multi-tone (DMT) communications system comprising:

receiving a standard pilot tone generated and transmitted by an associated far-end transmission unit along with other signal streams at a particular receiver;

converting the plurality of received signals through an analog to digital converter (ADC) to create a digital signal stream;

detecting a cyclic prefix in the digital signal stream;

using the digital signal stream with the cyclic prefix portion removed to generate an average pilot phase error using a discrete Fourier transform (DFT);

applying the average pilot phase error to the input of a timing recovery circuit to create a frequency correction signal; and

using the frequency correction signal to modify the sampling time of the ADC.

12. (Previously presented) The method of claim 11, further comprising:

synchronizing a digital to analog converter (DAC) in the transmitting path by using a sampling clock derived from the ADC.

13. (Original) A digital signal processor configured to apply the method of claim 1.

14. (Previously presented) A digital signal processor configured to compensate for the offset in phase error on a received pilot tone by sending a signal to a timing recovery circuit based upon a received signal segment in a discrete multi-tone (DMT) system initialization sequence; wherein the received signal segment comprises REVERB and SEGUE segments that have been generated by a pseudo-random pattern generator using an initial pattern that minimizes the pilot tone phase offsets in both segments.

15. (Original) The digital signal processor of claim 14, wherein the phase error compensation is accomplished with a state machine.

16. (Previously presented) A digital signal processor configured to detect a cyclic prefix from a received digital signal stream at an input to a timing recovery circuit and apply a signal of substantially zero amplitude to the timing recovery circuit when the cyclic prefix is present.

17. (Previously Presented) The digital signal processor of claim 16, wherein the digital signal processor is further configured to perform a time-domain equalization on ~~a~~ the received digital data stream.

18-20. (Canceled)

21. (Previously presented) A system for timing recovery in a discrete multi-tone communications system comprising:

an analog to digital converter (ADC) configured to create a digital representation of the received signal;

a timing recovery circuit in communication with the ADC configured to receive the received signal and to apply a control signal to the ADC, wherein the received signal sample stream is synchronized for further processing at a rate compatible with that of a source transmission.; and

a symbol synchronizer in communication with the ADC configured to determine when the data stream contains a cyclic prefix, the symbol synchronizer further configured to remove the received signal from the timing recovery circuit input when the cyclic prefix is present.

22. (Original) The system of claim 21, further comprising:

a sampling clock in communication with the analog to digital converter, the sampling clock in further communication with a digital to analog converter (DAC) in the transmitting path for synchronizing data transmitted in the reverse direction to the far-end transmission unit.

23. (Previously presented) A system for timing recovery in a discrete multi-tone communications system comprising:

an analog to digital converter (ADC) configured to create a digital representation of the received signal;

an equalizer in communication with the ADC, the equalizer configured to perform a time-domain equalization on the received signal;

a timing recovery circuit in communication with the ADC and the equalizer configured to receive the received signal and to apply a control signal to the ADC, wherein the received signal sample stream is synchronized for further processing at a rate compatible with that of a source transmission; and

a symbol synchronizer in communication with the ADC configured to determine when the signal stream contains a cyclic prefix, the symbol synchronizer further configured to remove the time-domain equalized signal from the timing recovery circuit input when the cyclic prefix is present.

24. (Original) The system of claim 23, further comprising:

a sampling clock in communication with the analog to digital converter , the sampling clock in further communication with a digital to analog converter (DAC) in the transmitting path for synchronizing signal transmitted in the reverse direction to the far-end transmission unit.

25. (Previously presented) A system for timing recovery in a discrete multi-tone communications system comprising:

an analog to digital converter (ADC) configured to create a digital representation of the received signal;

an equalizer in communication with the ADC, the equalizer configured to perform a time-domain equalization on the received signal;

a symbol synchronizer in communication with the ADC configured to remove a cyclic prefix from the signal sample stream;

a discrete Fourier transform (DFT) in communication with both the equalizer and the symbol synchronizer, the DFT configured to convert the time-equalized received signal and to generate a pilot tone phase error estimate signal;

a timing recovery circuit in communication with the ADC and the DFT configured to receive the pilot tone phase error estimate and to apply a control signal to the ADC, wherein the received signal sample stream is synchronized for further processing at a rate compatible with that of a source transmission.

26. (Original) The system of claim 25, further comprising:

a sampling clock in communication with the analog to digital converter, the sampling clock in further communication with a digital to analog converter (DAC) in the transmitting path for synchronizing signal transmitted in the reverse direction to the far-end transmission unit.

27. (Canceled).

28. (Previously presented) A system for timing recovery at the receiver in a discrete multi-tone (DMT) communications system comprising:

means for receiving a standard pilot tone and far-end signal from an associated far-end transmission;

means for converting the plurality of received signals from analog to digital signals;

means for detecting a cyclic prefix in the received far-end signal;

means for removing the cyclic prefix in the received far-end signal;

means for generating an average pilot phase error using a discrete Fourier transform (DFT); and

means for applying the average pilot phase error to the input of a timing recovery circuit to create a frequency correction signal; and

means for using the frequency correction signal to modify the sampling rate of the analog to digital conversion.

29. (Previously Presented) A system for timing recovery at the receiver in a discrete multi-tone (DMT) communications system comprising:

means for receiving a standard pilot tone along with a plurality of signals at this particular receiver from a far-end signal;

means for converting the plurality of signals from analog to digital signals;

means for performing a time-domain equalization on the far-end signal;

means for detecting a cyclic prefix in the far-end signal;

means for zeroing out the equalized digital signal from the input to a phase locked-loop while the cyclic prefix is present in the received signal to create frequency correction signal; and

means for using the frequency correction signal to modify the sampling rate of the analog to digital conversion.

30. (Previously presented) A system for timing recovery at the receiver in a discrete multi-tone (DMT) communications system comprising:

means for receiving a far-end signal along with a plurality of signals at the receiver;

means for converting the plurality of received signals from an analog to a digital format;

means for detecting <u>a</u> cyclic prefix in the far-end signal;

means for zeroing out the far-end signal when the cyclic prefix is present from the input to a timing recovery circuit; and

means for using the phase locked-loop output to modify the sampling rate of the analog to digital conversion.

31. (Previously Presented) The method of claim 7, further comprising: performing a time-domain equalization on the received digital signal stream.